

## Automotive-grade N-channel 40 V, 3.0 mΩ typ., 80 A STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data

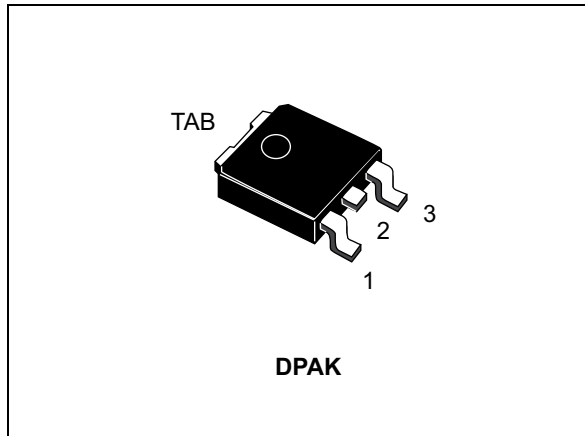
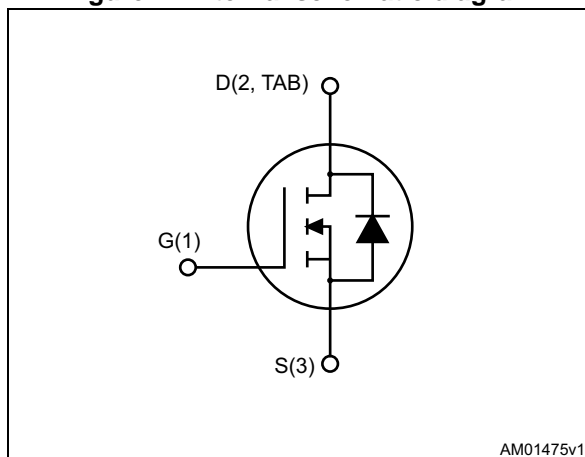


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STD130N4F6AG	40 V	3.6 mΩ	80 A

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STD130N4F6AG	130N4F6	DPAK	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	80	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	143	W
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature		

1. Current limited by package.
2. Pulse width limited by safe operating area.

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.05	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max <sup>(1)</sup>	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> 2 oz. Cu board.

**Table 4. Thermal resistance**

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not-repetitive	80	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	386	mJ

1. Pulse width limited by  $T_j$  max
2. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 80\text{ A}$ ,  $V_{DD} = 25\text{ V}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 5. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage ( $V_{GS} = 0$ )	$I_D = 250\ \mu\text{A}$	40			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 20\ \text{V}$			1	$\mu\text{A}$
		$V_{DS} = 20\ \text{V}, T_C = 125\text{ °C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}, I_D = 40\ \text{A}$		3.0	3.6	m $\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\ \text{V}, f = 1\ \text{MHz}, V_{GS} = 0\ \text{V}$	-	4260	-	pF
$C_{oss}$	Output capacitance		-	635	-	pF
$C_{riss}$	Reverse transfer capacitance		-	308	-	pF
$Q_g$	Total gate charge	$V_{DD} = 20\ \text{V}, I_D = 80\ \text{A}$	-	70	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\ \text{V}$	-	20	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 14)	-	18	-	nC
$R_G$	Intrinsic gate resistance	$f = 1\ \text{MHz}, I_D = 0$	-	1.5	-	$\Omega$

**Table 7. Switching on/off (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\ \text{V}, I_D = 40\ \text{A}, R_G = 4.7\ \Omega, V_{GS} = 10\ \text{V}$ (see Figure 15)	-	19.5	-	ns
$t_r$	Rise time		-	62.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	58	-	ns
$t_f$	Fall time		-	19.5	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 40 \text{ A}$ , $V_{GS} = 0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 80 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 32 \text{ V}$ <i>(see Figure 17)</i>	-	41		ns
$Q_{rr}$	Reverse recovery charge		-	58		nC
$I_{RRM}$	Reverse recovery current		-	2.8		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

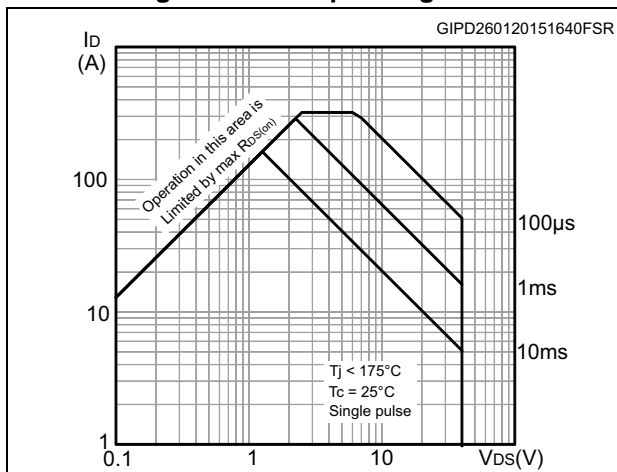


Figure 3. Thermal impedance

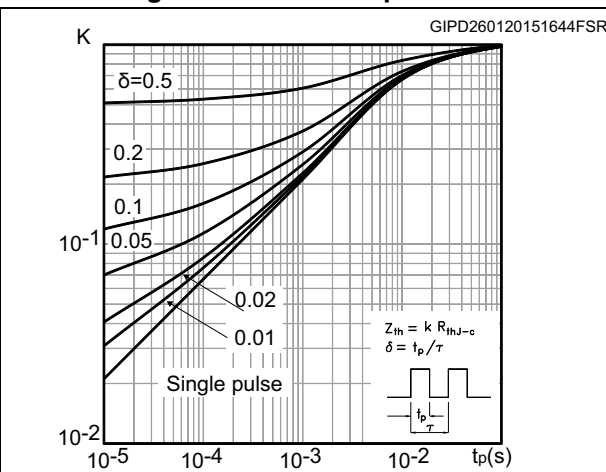


Figure 4. Output characteristics

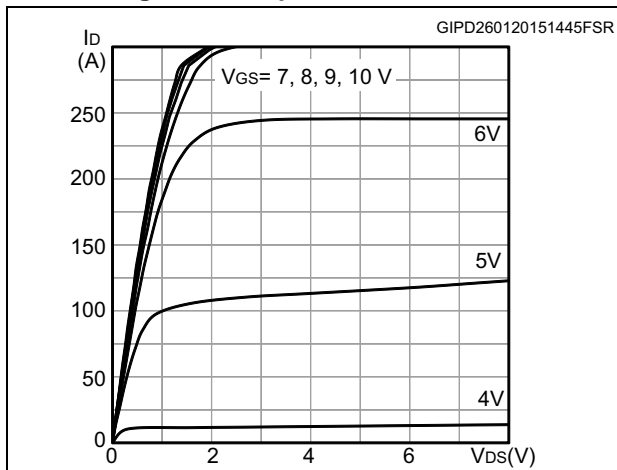


Figure 5. Transfer characteristics

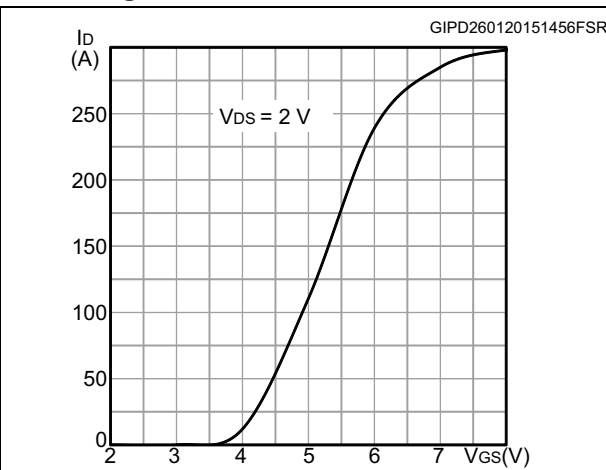


Figure 6. Normalized gate threshold voltage vs. temperature

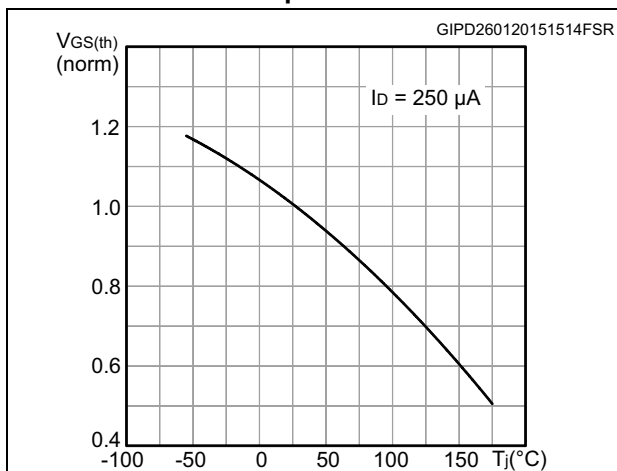


Figure 7. Normalized  $V_{(BR)DSS}$  vs. temperature

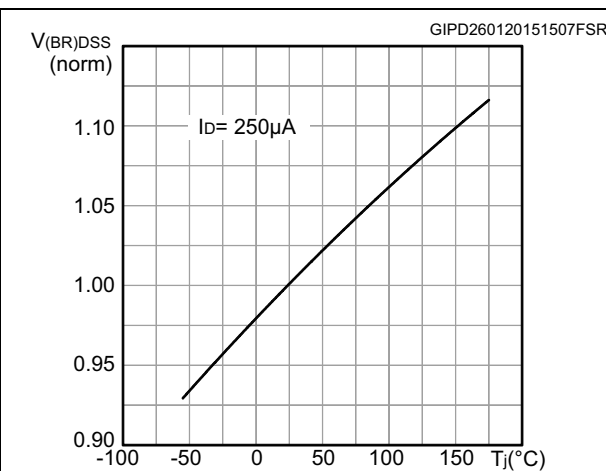


Figure 8. Static drain-source on-resistance

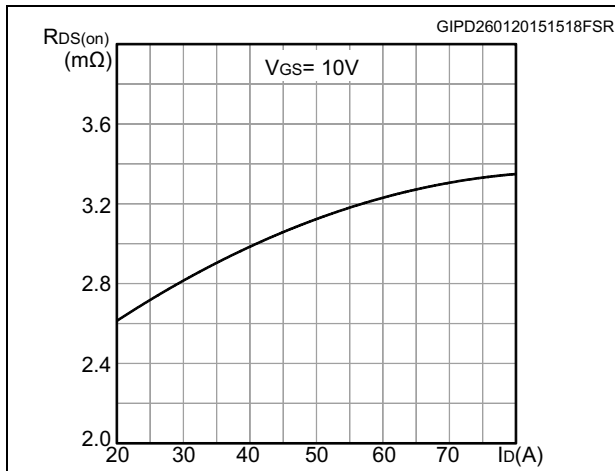


Figure 9. Normalized on-resistance vs. temperature

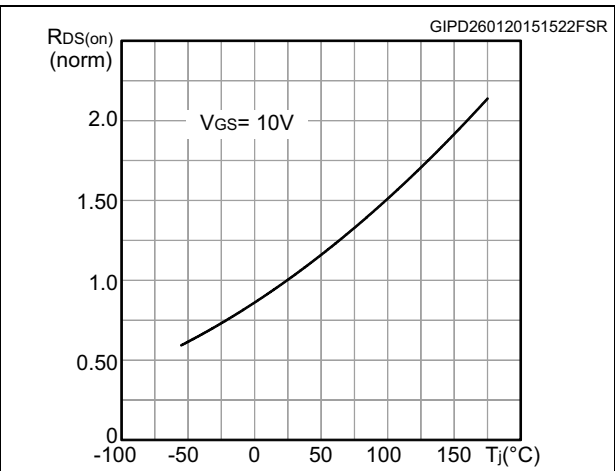


Figure 10. Gate charge vs. gate-source voltage

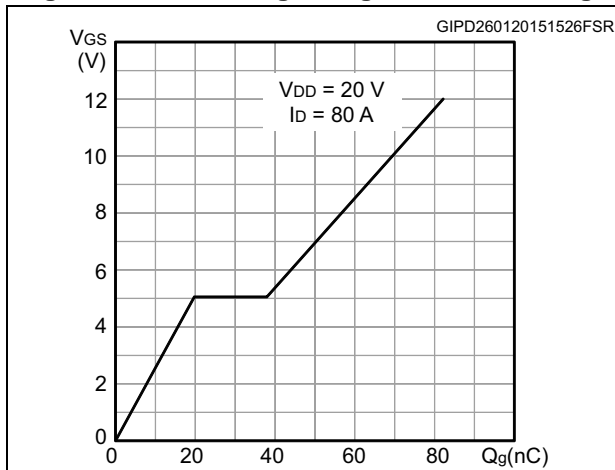


Figure 11. Capacitance variations

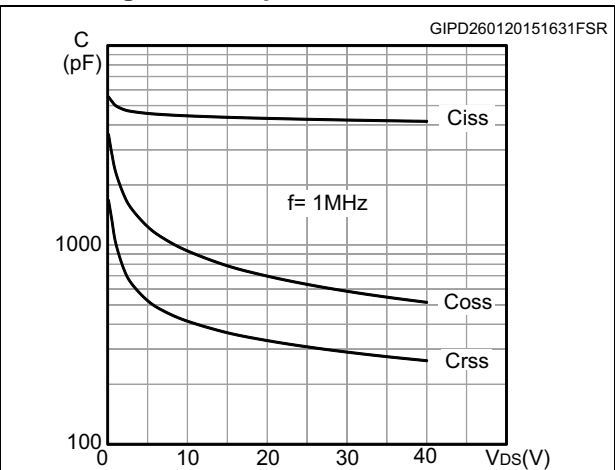
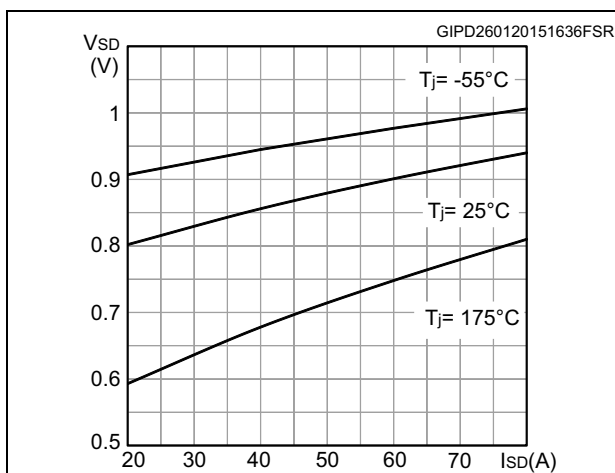


Figure 12. Source-drain diode forward characteristics



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

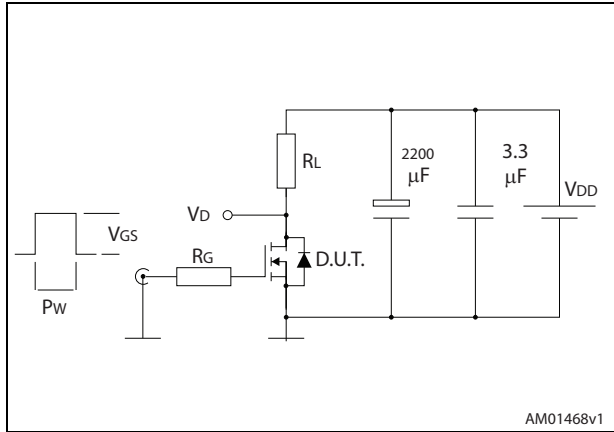


Figure 14. Gate charge test circuit

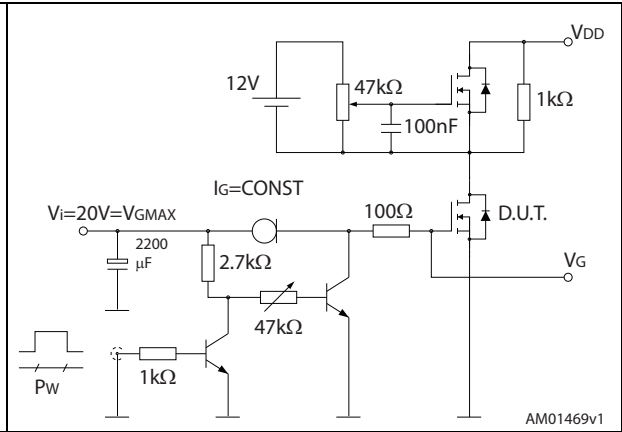


Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped Inductive load test circuit



Figure 17. Unclamped inductive waveform



Figure 18. Switching time waveform





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 19. DPAK (TO-252) type A2 drawing

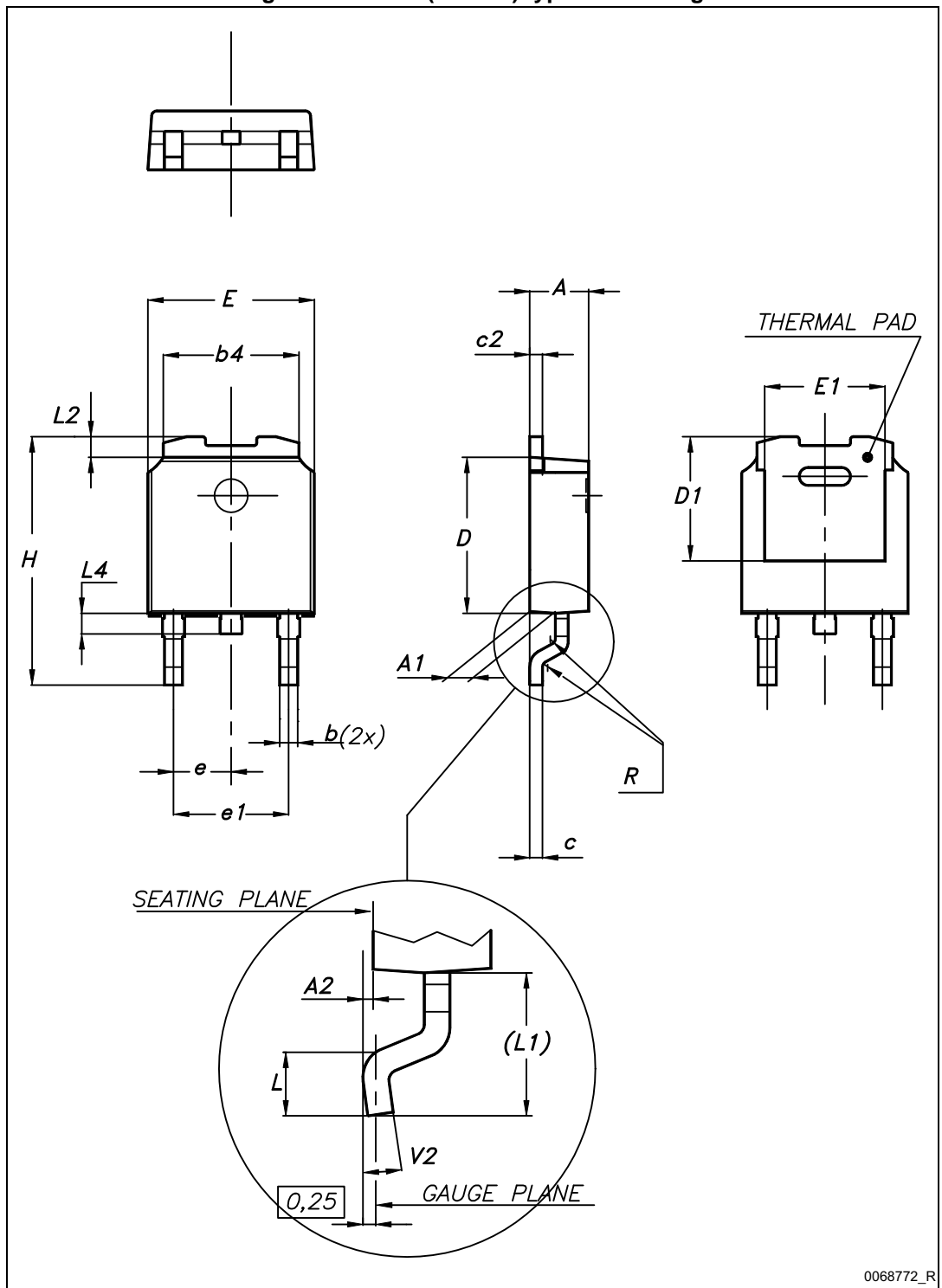
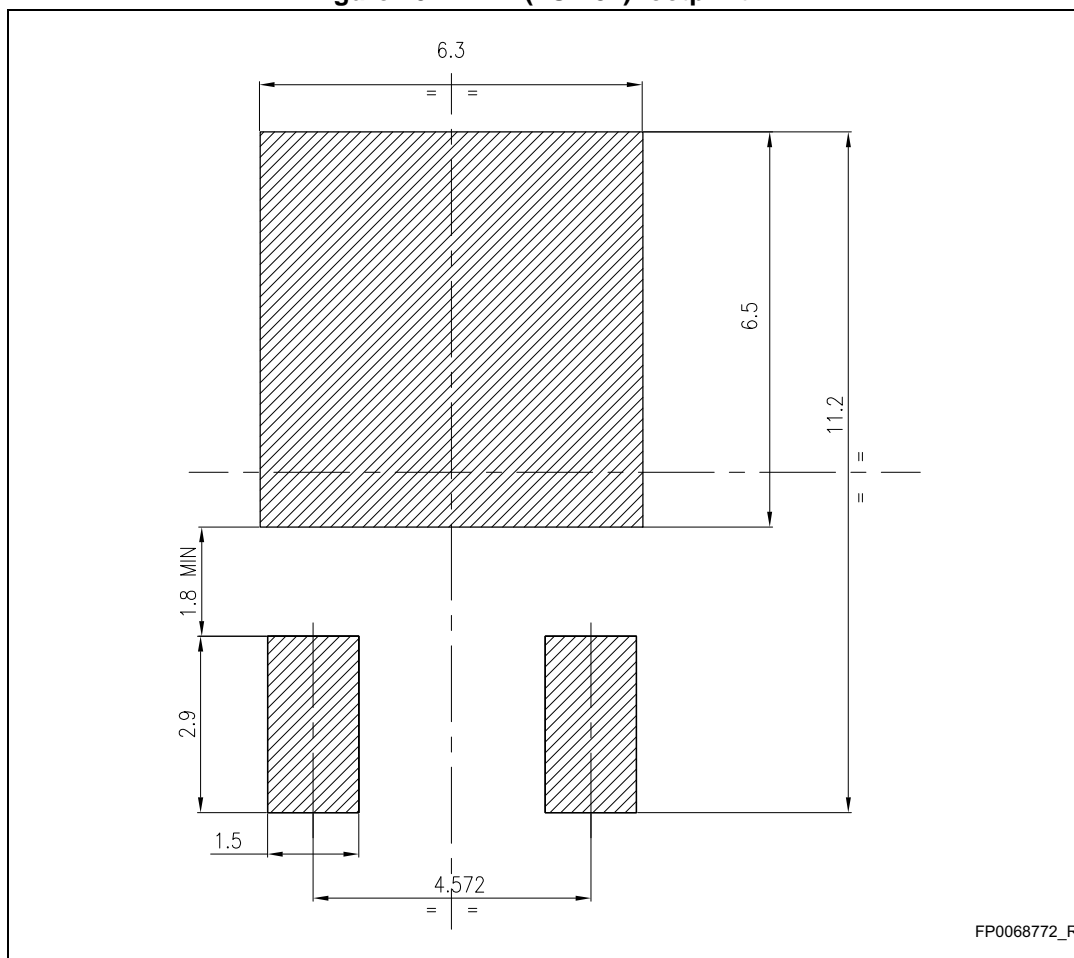


Table 9. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		5.20	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

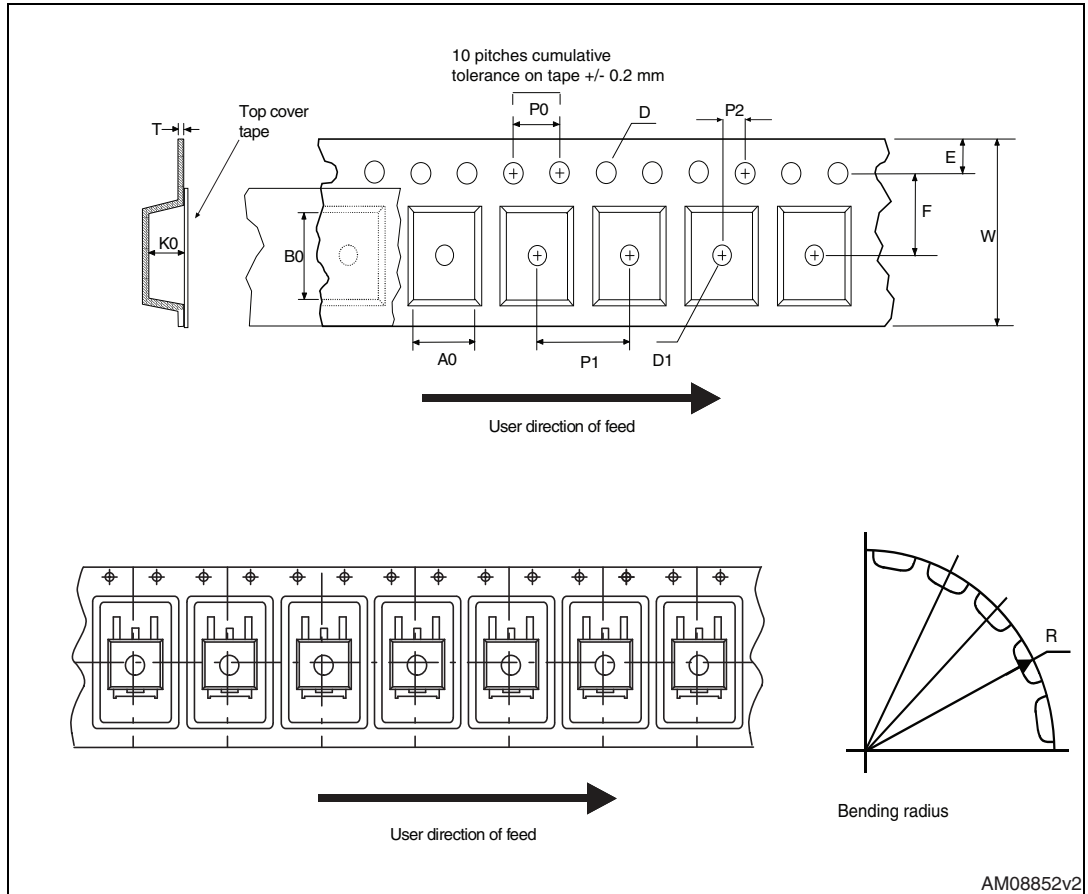
Figure 20. DPAK (TO-252) footprint (a)



a. All dimensions are in millimeters

# 5 Packaging mechanical data

Figure 21. Tape



AM08852v2

Figure 22. Reel

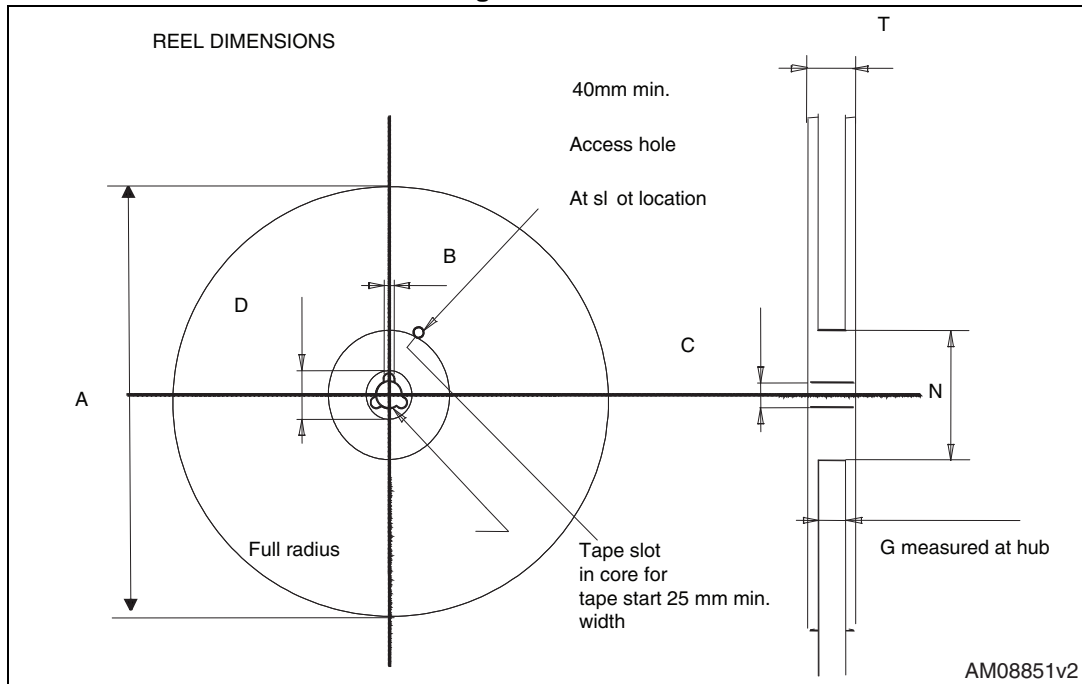


Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 6 Revision history

**Table 11. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
26-Jan-2015	1	First release
12-Feb-2015	2	Document status promoted from preliminary to production data. Updated title and description in cover page.

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